In the always @ statement in behavioural do we write all the inputs of the module in case of clock based sequential logic or only posedge clk is fine

=> At times only posedge clk is fine unless any other procedure mentioned such as asynchronous reset  
For clock-based sequential logic, only posedge clk (and optionally an asynchronous reset) is needed in the always @ sensitivity list. Including all inputs is unnecessary and may lead to unintended behavior.